

A Low Cost Digital Filter Bank for Ultra Wideband Radio

For further information,
please contact:

Professor Jugdutt (Jack) Singh

Director - Centre for Technology Infusion
Research Professor – Micro/Nanoelectronics
La Trobe University R&D Park
Victoria 3086
Australia

Email: CTI@latrobe.edu.au
Phone: +61 3 9479 5628
Fax: +61 3 9479 5209

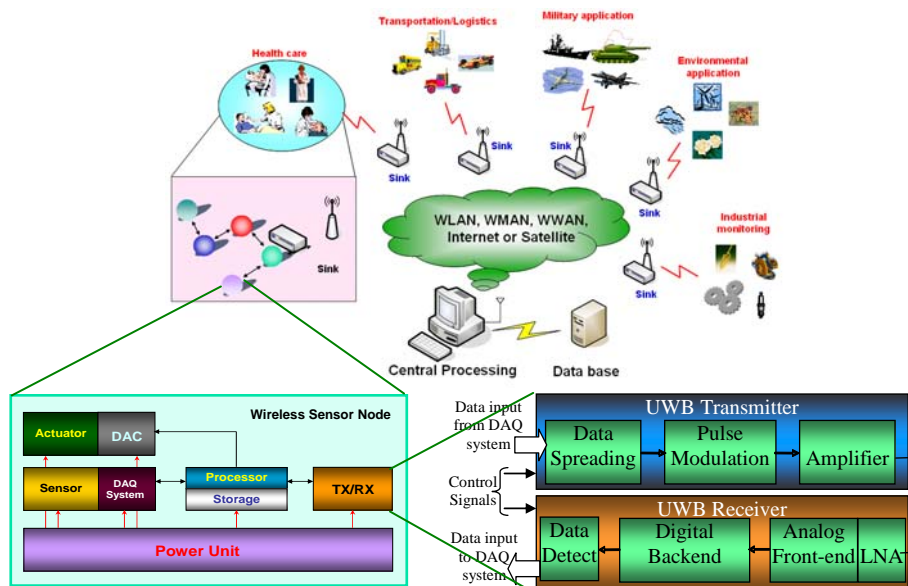
*“Fostering high-tech industry
development in ICT Sector”*

OVERVIEW

Wireless Sensor Networks (WSNs) open a new paradigm for extracting data from the environment and enable reliable monitoring/controlling for a large number of applications areas. They demand ultra low power consumption from the design components as they are battery operated. Various power reduction techniques and algorithms for the data acquisition block in WSN system are proposed in the literature.

PROJECT DESCRIPTION

The research involves reconfigurability analysis, design and implementation of an algorithm to achieve that, for power consumption reduction in the digital backend of a UWB receiver. Analysis shows that approximately 47% average power of the digital backend can be saved with reconfigurability, for a typical operating condition. Time delay is the important factor deciding the parallelism required.



Wireless Sensor Network and Ultra Wideband Receiver

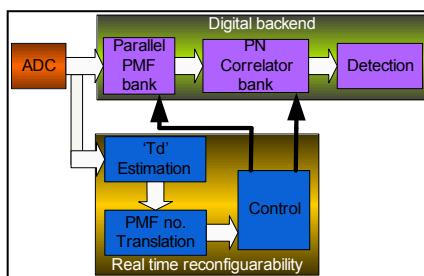
This research focuses on the application of Ultra Wideband (UWB) communication technology for the transceiver block in a WSN. Current digital UWB radio architecture uses significant parallelism in the digital backend during synchronisation operation which increases power consumption of the entire system. This research investigates the actual parallelism required and potential for power saving for different channel impulses and time delays that can be achieved by incorporating real time reconfigurability in digital backend of the UWB receiver. The research proposes an algorithm to achieve the real time reconfigurability in order to reduce power consumption.

Real time reconfigurability algorithm consists of time delay estimation, translation and control blocks. Estimation block estimates time delay of the received signal. Translation block converts these estimates into number of optimum parallel blocks required for processing and control block turns on/off the required blocks. This algorithm will facilitate intelligent adaptation of the receiver to changing condition and will contribute in reducing power consumption.

PERFORMANCE

The following table presents the performance summary of the digital filter design.

Parameter	Result
Core supply voltage	0.9 V
Filter Order	128
Operating frequency	7.81 MHz
Power Consumption	25.8µW
Technology	90nm
Core Area	47348.994µm ²



Real Time Reconfigurability

FURTHER INFORMATION

For more information, please contact
Email: CTI@latrobe.edu.au
Website: www.latrobe.edu.au/tech-infusion