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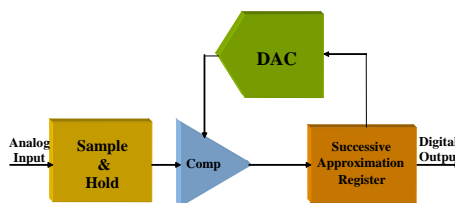
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OVERVIEW

In biomedical instrumentation, it is usually required to analyse and display biosignals obtained from sensors, which convert a physical measurement from human body to an electrical signal. Initially these signals were acquired, extracted and analysed using analog technology. However, since the digital signal processor has developed rapidly, engineers have turned to digital signal processing as a more advanced and convenient method. An Analog-to-Digital Converter (ADC) is, therefore, inevitably necessary as it will acquire and digitize analog signals for further analysis using the advanced digital signal processing technique. Biosignals, in nature, are low frequency but variable amplitude and frequently complex waveforms that occur in a very noisy environment. Therefore, it requires a high resolution ADC to preserve the integrity of the converted signals. Moreover, biomedical instruments require low power consumption and low complexity to reduce the size and cost as well as enable the next generation of portable biomedical instrument devices. Successive Approximation (SA) ADC is the most suitable architecture for biomedical applications. Traditional SA ADC consists of a Sample-and-Hold Circuit (SHC), a comparator, registers, logic controller and a Digital-to-Analog Converter (DAC) which is typically implemented using binary weighted technique. Due to the binary weight relation between the various capacitors or resistors used in the DAC, the SA ADC die size and power consumption drastically increases with the increase in resolution.

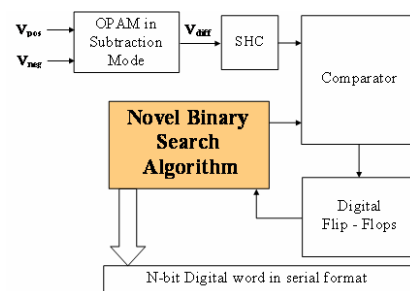


SA ADC ARCHITECTURE

PROJECT DESCRIPTION

In this project, a novel binary search algorithm is proposed to replace the conventional DAC in a traditional SA ADC architecture to significantly reduce the system area and power consumption. The proposed ADC architecture comprises of an Operational Amplifier (OPAM) in subtraction mode, a SHC, a comparator, a digital flip-flop (FF), which acts as a storage device for the comparator output, and the novel binary search algorithm block. The search algorithm searches for the appropriate reference voltage at each clock cycle depending on the input voltage signal and the output of the comparator, and thus the final digital output code is available after the Nth comparison (for N-bit resolution).

The proposed ADC is designed to operate in differential mode, thus, the positive input voltage (V_{pos}) is subtracted by the negative input voltage (V_{neg}) and the residue voltage (V_{diff}) is fed to the SHC.



NOVEL ULTRA LOW POWER ADC

The proposed ultra low power ADC is a variable-resolution architecture since the same hardware architecture can be used to obtain different output resolution. The proposed ADC architecture also eliminates the need for resistors and a high current voltage reference source as required in the sub-DAC in the traditional SA ADC. Instead, it employs an analog flip-flop, which acts as a storage device for the tracing voltage, and OPAM-based analog subtraction and addition blocks. Another advantage of the proposed ADC structure is that the digital logic is minimised to a single flip-flop. This eliminates numerous cross-talks between the analog and digital components and significantly reduces the complexity of the system layout process.

PERFORMANCE

The following table presents the performance summary of the ADC design.

Parameter	Result
Core supply voltage	2 V
Maximum resolution	16 bits
Max. frequency@16-bits	200Hz
Power Consumption @200Hz @ 16 bits resolution	22.2µW
Technology	0.18-micron CMOS
Core Area	0.1mm ²
DNL	≤ ±0.5LSB
INL	≤ ±0.3LSB

FURTHER INFORMATION

For more information, please contact
 Email: CTI@latrobe.edu.au
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