

**DEPARTMENT OF ELECTRONIC ENGINEERING**

**Unit Quality Assurance Report**

**YEAR:** 2005  
**SEMESTER:** 1st  
**UNIT CODE:** ELE51TAV  
**UNIT TITLE:** Test and Verification  
**LECTURER(S):** Snezana Markovic  
**CLASS SIZE:** 5

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**UNIT OBJECTIVES:**

The aim of the subject is to encourage the development EDA test and verification knowledge and skills pertinent to modern industry practice. Since 70 % design effort goes to verification the aim is to expose students to differences and importance of verification processes and techniques used to minimize costs and optimize development process.

**SURVEY RESULTS AND ANALYSIS OF INDIVIDUAL QUESTIONS:**

Only five surveys received – hence no detailed analysis of statistical information. Of the surveys received, four rated the unit as “Good” and one rated the unit as “Satisfactory”. Responses to other questions were along similar lines. Written suggestions for improvements focused on the laboratory classes. In particular it would appear that some operational (software set up) problems effected the running of some laboratory classes. More practical examples of testing techniques were encouraged.

**DISCUSSION AND RECOMMENDATIONS REFERRING TO UNIT OBJECTIVES AND SURVEY RESULTS:**

Only five surveys received – no statistical plots. Hard gauge an accurate assessment of student opinion due to limited of survey responses. However, it would appear that this unit is reasonably effective in meeting its objectives. Based on the responses it would appear that the lecture content is good. But, improvement could be made in the laboratory work – partly through improving software tool set up, but also by expanding practical examples/tasks.

**RECOMMENDATION(S) FOR FOLLOWING YEAR:**

- Improve software tool set up;
- Check lab tasks work on current software environment;
- Expand practical examples/tasks were appropriate.