

Industry Sponsored Projects for 2007

Department of Electronic Engineering
La Trobe University

The following is a list of industry sponsored projects for 2007. The list is subject to change and will be updated when necessary. Industry projects are part of final year projects (ELE4EPA & ELE4EPB). Due to the commercialisation nature of these projects, stringent selection is expected. Academic excellence (minimum 70%), high commitment and responsibility are required to perform these projects. Application forms are available from Department of Electronic Engineering Reception (SW4 432).

1.

Project Title: XML Reconfigurable Ports for HMI (AutoCRC project code: UG406)

Sponsoring Company: AutoCRC

Abstract: Design and develop a XML program with reconfigurable input/output ports for the RAP HMI microprocessor board.

Contact Person: John Devlin (j.devlin@latrobe.edu.au)

2.

Project Title: Traffic Simulation - CBD (AutoCRC project code: UG706)

Sponsoring Company: AutoCRC

Abstract: Centralised car control Vic roads CBD

Analysis of Traffic congestion and fuel economy improvements possible via centrally controlled by-wire vehicles in CBD, main roads etc.

Initial analysis into technical constraints so that appropriate model assumptions are used.

Contact Person: John Devlin (j.devlin@latrobe.edu.au)

3.

Project Title: Emulator for CAN bus to support software development, verification and error analysis (AutoCRC project code: UG4606)

Sponsoring Company: AutoCRC

Abstract: Robust in-Vehicle Software Development:

This capability (tool) will allow project developing technology on or for the CAN bus (could be extended for other bus technologies).

This testing and development capability will speed up redevelopment and make the software more robust.

Contact Person: Jim Whittington (j.whittington@latrobe.edu.au)

4.

Project Title: API interface between a Debugging Utility and an In-Circuit-Emulator

Sponsoring Company: Softronics www.softronx.com

Abstract: The API function is to take the commands from the Application and process this so that these commands can be pass onto an embedded device.

This project is to implement an API to interface between a PC based Software Debugger and an In-Circuit-Emulator.

The API will consist of a number of function calls which can be accessed via the Debugging Software and are executed on the In-Circuit-Emulator.

Based upon last years works, the design requires an enhancement so as to enable additional functionality.

The API is clearly defined. The Debugger is based upon freely available open source and is well defined and understood.

The In-Circuit-Emulator interfaces are well documented and understood.

The testing procedure will need to tailor these components to verify the testability outcomes.
You will show your creativity to address special issues as they arise.

Required Student Skills: Strong GDB/GNU and C++ skills would be beneficial but not mandatory.
An interest in interfacing hardware through APIs to the PC and implementation methodologies as applied to embedded systems.

Contact Person: Jim Whittington (j.whittington@latrobe.edu.au)

5.

Project Title: API FPGA In Circuit Emulator for ARM RISC and TI DSP (IC Design)

Sponsoring Company: Softronics www.softronx.com

Abstract: This project is to build an In-Circuit-Emulator (ICE) using an FPGA.

The ICE interfaces between the PC and its Software Debugger and an embedded Micro Processor, in this case an ARM RISC or a TI DSP.

The ICE's function is to take JTAG (IEEE1149.1) commands from the PC application and process this and pass this onto an embedded device and also the converse.

The design is loaded into an FPGA and tested by connecting the design to a PC via its USB interface. Using both the USB interface and device drivers which are readily available, the testing procedure will need to tailor these components to verify the testability outcomes.

You will show your creativity to address special issues as they arise.

Required Student Skills: Strong VHDL /Verilog skills would be beneficial but not mandatory.
An interest in interfacing FPGAs to the PC and implementation methodologies as applied to embedded systems.

Contact Person: Jim Whittington (j.whittington@latrobe.edu.au)

6.

Project Title: Link Layer Controller - Integrated Circuit Design (FPGA)

Sponsoring Company: Softronics www.softronx.com

Abstract: This project is to build a IEEE 1394B (Firewire) 800MBit/s Link Layer Controller.

The Link Layer Controller interfaces between Physical Layer device and an embedded (existing) controller.

The Link Layer Controller's function is to take the raw data from the Physical Layer Interface chip and process this and pass this onto an embedded device.

Based upon freely available IP for the IEEE 1394A (400 MBit/s) the design requires an enhancement so as to enable the 1394B standard to be implemented.

The design is loaded into an FPGA and tested by connecting the design to a PC via its 1394B interface (a PCI Card interface). Using both PCI cards and device drivers which are readily available, the testing procedure will need to tailor these components to verify the testability outcomes.

You will show your creativity to address special issues as they arise.

Required Student Skills: Strong VHDL /Verilog skills would be beneficial but not mandatory.
An interest in interfacing FPGAs to the PC and implementation methodologies as applied to embedded systems.

Contact Person: Jim Whittington (j.whittington@latrobe.edu.au)

7.

Project Title: Fuzzy Controller for a Power Supply

Sponsoring Company: M. Brodribb Pty Ltd www.brodribb.com.au

Abstract: Impressed current cathodic protection systems operate by passing current from an anode through a conductive path (soil, water etc) and to the protected structure to prevent rusting. If the structure is under-protected, rusting will occur. If the structure is over-protected then hydrogen gas may be evolved from the steel, leading to embrittlement of the steel and

delamination of the protective coating. The electrochemical potential is usually measured by a reference electrode with one end connected to the protected structure.

We propose that it is possible to make a controller that combines protection rules to make up a fuzzy control system. The controller would determine how close to protection each of the criteria were and provide a linear dc output to our phase control system. The controller would also take other priority signals in, such as maximum voltage and current limits and recognise these as hard limits. The controller would interface with other parts of the rectifier so that off potential and potential shift can be measured by switching off the rectifier. The controller would also recognise when over protection was occurring. The weighting of each rule would be adjustable in software.

Contact Person: Jim Royston (j.royston@latrobe.edu.au)

8 & 9.

Project 8: Battery charge and control system (**This project has been taken by Bernard McCrohan**)

Project 9: Battery communication package

Sponsoring Company: DSTO

Abstract: The Defence Science and Technology Organisation (DSTO) use a three cell lithium battery to power the Uninhabited Aerial Vehicles (UAV). Three of batteries are used in series to provide the required voltage of 33.3V. These batteries are required to be charged at 2A and discharged up to a rate of 100A.

The batteries are currently kept within a small charge of each other by using a small circuit created in house at DSTO. It measures the voltage of the cells and discharges the other cells to the voltage of the lowest cell. The accuracy of this device is unknown but a desired difference is +/- 0.01V.

It has been found that during flight one of the cells in any of the three batteries reaches its break down voltage. When this occurs, the voltage avalanches and effectively creates an open circuit. The risk involved in such an event spans from battery replacement, battery replacement and other damaged components to total loss of aircraft. Even in the event of the lowest risk factor occurring, it still financially justifies the development of a battery management system

What DSTO require is an effective battery management system that provides accurate information to the aircraft operator so the UAV can be returned to base without damage to the battery packs or the vehicle.

These requirements can be broken into two separate projects:

- To develop a battery management system that protects the batteries without compromising the safety of the vehicle.
- Provide performance information of the batteries to the user which may effect the safe operation or performance of the vehicle.

Contact Person: John Devlin (j.devlin@latrobe.edu.au)

10. (Choose one project from the following three)

Projects: (1) Peak to average ratio (PAR) reduction for an OFDM system

(2) Time and frequency tracking for an OFDM system

(3) Turbo decoder for very high T-put

Sponsoring Company: 3G Mobile R&D Division, NEC Australia

Abstract: The aim of the projects is to search available literature and select an implementable scheme with good performance, then confirm the performance of the selected scheme through modelling.

Required Student Skills: Wireless communication backgrounds (particularly OFDM technology)

Literature search and analysis Algorithm development and evaluation
System modelling (Matlab or C/C++)

Contact Person: Song Wang (Song.Wang@latrobe.edu.au)

11.

Project Title:

Development of LED video display panel

Abstract:

This project is specifically targeted at developing modular LED video display panels capable of being connected together to form a large display. The display panels will be able to display full RGB colour, and will be controlled by an FPGA which has the dual function of reading in the data to be displayed from a remote computer, and sending the correct signals to the LED panels to display the downloaded image.

It is proposed to design the circuit such that the same FPGA module can be used for both the controller and the display panels. This requires the following hardware::

1. A control board
2. A separate LED Display board

In addition to this there are a number of software components which need to be completed:

1. Communication between control FPGA and computer
2. Division of image stored in control FPGA into individual images which are sent to each separate display panel
3. Communication of sub-images to separate LED Display panels
4. Generation of correct signals on each separate LED Display panel to display the desired image.

Required Student Skills:

- Good knowledge of C/C++, digital design and communication system fundamentals
- FPGA design experience using VHDL

Resources Required: Access to workstation with FPGA development tools

Company Support: Technical supervision
FPGA Development kit (Altera or Xilinx)

Special Requirements: None

Delivery Timeframes: November 2007

Sponsoring Company: Victorian Machine Vision

Contact Person: Jim Whittington (j.whittington@latrobe.edu.au)

12. (Project information on the next page)

Project Title:

Development of LED based Mini Projector

Abstract:

This project is specifically targeted at developing a highly compact LED based projector that uses a single miniature LCD panels, and the light of red, green, and blue LEDs collimated and homogenized using doped light guides to provide efficient mixing. This creates a light efficient projector highly miniaturized projector capable of projecting WVGA images at video speed.

This design involves the following hardware development

1. Design of LED control board
2. Design of interface circuitry to output the desired video signal to the LCD
3. Design and testing of light concentrators (which have the dual purpose of concentrating the light, and mixing the RGB components)

In addition to this there are a number of software components which need to be completed:

1. Communication between LED control board and PC
2. Communication between LCD control and PC

Required Student Skills:

- Good knowledge of C/C++, digital design and communication system fundamentals
- FPGA design experience using VHDL

Resources Required: Access to workstation with FPGA development tools

Company Support: Technical supervision
FPGA Development kit (Altera or Xilinx)

Special Requirements: None

Delivery Timeframes: November 2007

Sponsoring Company: Victorian Machine Vision

Contact Person: Jim Whittington (j.whittington@latrobe.edu.au)